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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In Re Application of:	
Tu et al.	Group Art Unit: 2822
Serial No.: 10/822,197	Examiner: Thomas, Toniae M.
Filed: April 4, 2004	Confirmation No.: 2371
For: **Metal (MIM) Capacitor Structure**	TKHR Docket: 252016-2430 Top-Team: 0503-A30753US

CERTIFICATE OF FACSIMILE TRANSMISSION UNDER 37 CFR §1.8

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November 18, 2005
Date

Hui Chin Barnhill

AMENDMENT AND RESPONSE TO OFFICE ACTION

Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450

Sir:

The Office Action mailed September 9, 2005 has been carefully considered. In response thereto, please enter the following amendments and consider the following remarks.

AMENDMENTS

In the Claims

Claims 1-32 (canceled).

Claim 33 (Original): An embedded DRAM and capacitor structure device comprising:

trenched capacitors in two twisted trenches through an insulating layer in a memory area of an integrated circuit wherein said two twisted trenches are mirror images of each other and wherein each capacitor in a first of said two twisted trenches is horizontally aligned with a capacitor in a second of said two twisted trenches to form pairs of capacitors wherein said pairs of capacitors are separated from each other horizontally by a first or a second distance wherein said first distance is greater than said second distance;

a bit line contact in said memory area through said insulating layer to a bit line wherein said bit line contact lies between said two twisted trenches and in a horizontal line with one capacitor pair wherein said one capacitor pair has said first separation distance and adjacent capacitor pairs have said second separation distance; and

first line metal contacts in a logic area of said integrated circuit;

wherein said bit line contact and said first line metal contacts are no higher vertically than said trenched capacitors.

Claim 34 (Currently amended): A DRAM structure comprising:

trenched capacitors in a two trenches through an insulating layer in a memory area, wherein each of said trenched capacitors comprises a bottom electrode lining an opening in said insulating layer, a capacitor dielectric layer disposed on said bottom electrode, and a top electrode disposed on said capacitor dielectric layer wherein an opening remains in said top electrode within said corresponding trench; and

a conductive line disposed on said top electrodes and filling inside said openings and said trenches continuously wherein said conductive line is no higher vertically than said top electrode.

Claim 35 (Original): The DRAM structure according to claim 34, further comprising a bit line contact in said memory area through said insulating layer to a bit line.

Claim 36 (Original): The DRAM structure according to claim 34, wherein said bit line contact is no higher vertically than said trenched capacitors.

Claim 37 (Original): The DRAM structure according to claim 34, wherein said insulating layer is a laminated layer comprising a stop layer, an insulating oxide layer, a silicon carbide layer, and a low-K layer disposed sequentially over said memory area.

Claim 38 (Original): The DRAM structure according to claim 37, wherein said trench is formed in said low-K layer and does not exceed said silicon carbide layer.

Claim 39 (Original): The DRAM structure according to claim 37, wherein said bottom electrode is in contact with said stop layer.

Claim 40 (Original): The DRAM structure according to claim 34, wherein said trench is twisted-shaped.

Claim 41 (Original): A DRAM structure comprising:

trenched capacitors in two trenches respectively and continuously in contact with said trenched capacitors;

two conductive bit lines filling said two trenches respectively and continuously in contact with said trenched capacitors; and

a bit line contact in said memory area through said insulating layer to a bit line wherein said bit line contact lies between said two trenches;

wherein said bit line contact is no higher vertically than said trench capacitors.

Claim 42 (Original): The DRAM structure according to claim 41, wherein each of said trenched capacitors comprises a bottom electrode layer lining an opening in said insulating layer, a capacitor dielectric layer disposed on said bottom electrode, and a top electrode layer disposed on said capacitor dielectric layer.

Claim 43 (Original): The DRAM structure according to claim 42, wherein said conductive lines are disposed on said top electrode layers and substantially filling inside said openings and said trenches respectively wherein said conductive lines are no higher vertically than said top electrode layers.

Claim 44 (Original): The DRAM structure according to claim 42, wherein said insulating layer is a laminated layer comprising a stop layer, an insulating oxide layer, a silicon carbide layer, and a low-K layer disposed sequentially over said memory area.

Claim 45 (Original): The DRAM structure according to claim 44, wherein said trenches are formed in said low-K layer and does not exceed said silicon carbide layer.

Claim 46 (Original): The DRAM structure according to claim 44, wherein said bottom electrodes contact said stop layer.

Claim 47 (Original): The DRAM structure according to claim 41, wherein said trenches are twisted-shaped.

Claim 48 (canceled).

Claim 49 (Currently amended): ~~The embedded DRAM and capacitor structure device according to claim 48, further comprising~~ An embedded DRAM and capacitor structure device,

comprising:

trenched capacitors in two trenches through an insulating layer in a memory area of an integrated circuit;

two conductive lines filling said two trenches respectively and continuously in contact with said trenched capacitors;

a bit line contact in said memory area through said insulating layer to a bit line wherein said bit line contact lies between said two trenches; and

first line metal contacts in a logic area of said integrated circuit;

wherein said two conductive lines are no higher vertically than a top electrode of said trenched capacitors and said bit line contact and said first line metal contacts no higher vertically than said trenched capacitors.

Claim 50 (Currently amended): The embedded DRAM and capacitor structure device according to claim 4849, wherein said two trenches are twisted-shaped.

Claim 51 (Original): The embedded DRAM and capacitor structure device according to claim 50, wherein said two twisted trenches are mirror images of each other.

Claim 52 (Original): The embedded DRAM and capacitor structure device according to claim 50, wherein each capacitor in a first of said two twisted trenches is horizontally aligned with a capacitor in a second of said two twisted trenches to form pairs of capacitors wherein said pairs of capacitors are separated from each other horizontally by a first or a second distance wherein said first distance is greater than said second distance.

Claim 53 (Original): The embedded DRAM and capacitor structure device according to claim 52, wherein said bit line contact is in a horizontal line with one capacitor pair wherein said one capacitor pair has said first separation distance and adjacent capacitor pairs have said second separation distance.

REMARKS

The Examiner is thanked for the thorough examination of the present application, the allowance of claim 33, and the indication that claims 37-40, 43-47, and 49-53 contain allowable subject matter. The Office Action, however, rejected claims 34-36 under 35 U.S.C. 102(b). The Office Action also rejected claims 41, 42, and 48 under 35 U.S.C. 102(e).

Applicants have amended claim 34 to make certain minor editorial changes, and claim 48 is canceled. Claim 49 is amended to write it in independent form, including all of the limitations of the base claim. Claim 50 is amended to be dependent upon claim 49. No new matter is introduced into the application by these amendments.

Response to Rejections Under 35 U.S.C. 102(b)

Claims 34-36 were rejected under 35 U.S.C. 102(b) as allegedly anticipated by *Choi* (US 6,072,210). For at least the reasons set forth below, Applicants respectfully disagree.

The Office Action asserted that *Choi* (US 6,072,210) discloses a DRAM structure which comprises a conductive line 21 disposed on the top electrodes and filling inside the opening and the trench continuously, wherein the conductive line is no higher vertically than the top electrode. However, in *Choi*, the element 21 is a top plug layer or a plug (see col. 3, line 47-55). In other words, the element 21 is a conductive layer or a conductive plug, which is similar to a contact or via. Significantly, element 21 is not a conductive line as recited in claim 34 of the invention. As the element "a conductive line..." is not disclosed in *Choi* (US 6,072,210), the rejection of claim 34 under 35 U.S.C. 102(b) should be withdrawn.

In addition, the rejection of claims 35 and 36 under 35 U.S.C. 102(b) should also be withdrawn for at least the same reason, because of dependence thereof from claim 34.

Applicants therefore respectfully traverse the rejections under 35 U.S.C. 102(b) for at least the aforementioned reasons.

As claim 34 should be allowed, dependent claims 37-40 should be allowed as well.

Response to Rejections Under 35 U.S.C. 102(e)

Claims 41, 42 and 48 were rejected under 35 U.S.C. 102(e) as allegedly anticipated by *Chiang et al.* (US 6,656,785 B2).

The Office Action alleged that *Chiang et al.* (US 6,656,785 B2) discloses a DRAM structure comprising two conductive lines 180 filling the two trenches respectively and continuously and continuously in contact with the trenched capacitors, as recited in claim 41. In *Chiang et al.*, the element 180 is a conductive line filling the two trenches respectively and continuously and continuously in contact with the trenched capacitors but not two conductive lines. The conductive lines marked by Office Action are just conductive materials filling in the trenched capacitors and at most regarded as vias or contacts but not conductive lines. Since the claimed element "two conductive lines..." is not disclosed in *Chiang et al.*, the rejection of claim 41 under 35 U.S.C. 102(e) should be withdrawn. In addition, the rejection of claim 42 under 35 U.S.C. 102(e) should also be withdrawn for at least the same reason, because of its dependence from claim 41. Applicant therefore respectfully traverses the rejections under 35 U.S.C. 102(e) for at least the aforementioned reasons.

As claim 41 showed be allowed, claims 43-47 should be allowed for at least the same reason.

For at least the same reasons, Applicant submits that this application is now in condition for allowance. Prompt issuance of a Notice of Allowance is earnestly solicited.

CONCLUSION

In view of the foregoing, it is believed that all pending claims are in proper condition for allowance. If the Examiner believes that a telephone conference would expedite the examination of the above-identified patent application, the Examiner is invited to call the undersigned.

No fee is believed to be due in connection with this amendment and response to Office Action. If, however, any fee is believed to be due, you are hereby authorized to charge any such fee to deposit account No. 20-0778.

Respectfully submitted,

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